

Andrew Copper

Electronics Engineer

“Proven Manager, Practical and Organized”

415-867-8517
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San Francisco, CA 94114-2319

My career objective is to create additional value within an organization by utilizing my proven management experience and technical aptitude along with my practical and organizational insight.

I would bring to your company a wide range of skills, including proven management experience of small and medium-sized teams, and direct program management experience, with the ability to keep teams on track and within budget. Additionally, I possess a strong ability for problem-solving and crisis management. My engineering knowledge is broad, spanning the gamut from ASICs/SoCs to complete hardware solutions, and I am experienced in working with a product throughout its entire life cycle. I have excellent verbal, written, and presentation skills, and enjoy the opportunity to teach and train whenever possible. I am very comfortable working with people and customers, and consider it to be an essential element in my success.

I am confident that I would be a valuable asset to your company regardless of position, and would be an immediate “fit”. I love working for companies where my contributions have a direct impact to the success of the product and company. I am extremely goal-oriented, and success-driven. I relish new opportunities for growth.

I would welcome the prospect to further discuss any applicable positions with you. If you have questions or would like to schedule an interview, please contact me by phone at **415.867.8517**

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Resume

Executive Summary

Proven manager and experienced digital design developer, specializing in Design For Test (DFT) and Static Timing Analysis (STA), who is eager to learn new skills and meet new challenges. Self-directed team player who adds both practical and organizational insight to his team. Works well with customers. Excellent presentation skills with extensive classroom teaching and demo experience. Key troubleshooting resource across multiple organizations.

Skills

- **Management of small- to medium-sized cross-functional teams**
- **Budget-focused, and able to find practical solutions to problems**
- **Numerous scripting languages; Perl, TCL, CSH, C++/C, Visual Basic, Assembly Language, Verilog, VHDL, SQL**
- **Full project life-cycle experience and design automation**
- **Writing, editing, technical reviewer**
- **Technical training and presentation**
- **Technical committee membership (SNUG Technical Chair 2005-2008, ITC Technical paper reviewer)**

Tools Summary

Synopsys : Design Compiler, Physical Compiler, DFT Compiler, BSD Compiler, PrimeTime, VCS, TetraMAX, DFTMax, Formality

Mentor : FastScan, Testkompres, DFTAdvisor, BSDArchitect, Modelsim

LogicVision : LogicBIST, IC MemoryBIST

Virage : SMS, Integrator, STAR Builder

Cadence : VerilogXL, NCVerilog

Career Summary

Test Engineering Manager – Aquantia, Inc.

Director Test Technology – E L & Associates, Inc.

Staff Applications Engineer / Applications Manager – Azuro, Inc.

Senior Corporate Applications Engineer – Synopsys, Inc.

Senior Engineer – Texas Instruments, Inc.

Design Engineer – Oasis, Inc. (acquired by TI)

Development Engineer – Two Way TV Ltd.

Development Engineer – Switched Reluctance Drives Ltd.

Non Career Summary

President – Folsom Street Events

SNUG – Technical Chair (2005-2008) and Committee Member

ITC – Technical paper reviewer

Beverage Manager – Large Non-Profit Event San Francisco

Career Experience

2006-Present **Aquantia, Inc.** Milpitas, CA

Test Engineering Manager

- Manage a team of 5 (2 DFT Engineers, 2 Test Engineers, 1 Product Engineer)
- Responsible for all of the DFT Specifications, DFT Implementation, Test Engineering functions and initial production sampling
- Support SoC design including test logic design, full chip integration, and verification in full chip environments
- Support characterization / production / burn-in testing, which includes test pattern generation, test pattern bring-up, and failure analysis. (Verigy 93K, Verigy ZFP)
- Good knowledge of all DFT aspects such as scan test, memory test, JTAG./BSD including capability of using required tools (DFTMax, PT)
- Experienced with SoC design and production support
- Good working knowledge of back-end flow such as STA, layout
- Knowledge of CPU/bus architecture, memory controller, and high-speed interface modules (SERDES)
- Good knowledge of Test Engineering functions such as load board design, Test Program creation, Initial Yield analysis
- Created a SQL database with Perl interface for in-depth analysis of test results

2004-2006 **EL & Associates** Pleasanton, CA

Director Test Technology

- Director of the engineering team specializing in integrated solutions for Design-For-Test (DFT) and Design-For-Manufacturing (DFM) services for ASIC, SoC, and FPGA. Engaged with customers from the RTL phase to silicon prototype
- Specialized in design-for-test, crisis management, project management, as well as DFT compression technologies. Other key focus areas include PrimeTime static timing analysis, and complete methodology flows. Proven success on 90nm 40 million-plus gate designs, using Transition Delay Fault (TDF) testing, as well as Critical Path Analysis (CPA).

2003-2004 **Azuro, Inc.** San Jose, CA

Staff Applications Engineer / Applications Manager

- Led the applications team of 3 for this start-up EDA company, developing an innovative low-power technology using physical information
- Worked with the R&D team to specify and develop new functionality
- Provided front line customer support, training and presentations
- Coordinated the entire effort to host a suite at DAC 2004
- General technical go-to for all networking, phone, office and computer problems

2001-2003 **Synopsys, Inc.** Mountain View, CA

Senior Corporate Applications Engineer

- Member of the CAE team supporting the Synopsys DFT tools
- Using input from marketing and R&D, designed and created product demos, which I then presented at DAC, SNUG, and ITC
- Created the internal and external training on all DFT product tools: DFT Compiler, TetraMAX, SoCBIST, SoCTEST, and Physical Scan Synthesis
- Key contributor to the flagship SoCBIST product launch team;

- providing targeted on-site support, customer and AC training, and significant customer integration assistance
- Developed flow and methodology for physical scan synthesis, and became the point person for that tool

1997-2001 **Texas Instruments Inc.** San Jose, CA

Senior Engineer / Member Group Technical Staff

- Expert in both Mentor & Synopsys tools and flows. Acted as key contact in these areas, and advised on numerous designs. Specific accomplishments included:
 - Architected and implemented complete synthesis, static timing, scan and ATPG flows. This included cost analyses for various DFT alternatives and fault coverage analyses
 - Worked extensively with customers and with internal TI engineers. Provided individual mentoring and developed a central lessons-learned web site
 - Interacted independently with large customers with minimal assistance
 - Influenced the move to more efficient test methods, helping reduce time to market and total cost of test
 - Performed crisis management for complex ASICs with large DFT problems
 - Solved problems with RTL and clock tree structures
 - Developed complete training programs in general IC testability concepts and for tool-specific flows
- Member, Technical Program Committee for Texas Instruments Symposium on Test (TIST); presented several publications
- Elected to Member Group Technical Staff (MGTS), TI Technical Ladder

1996-1997 **Two Way TV, Ltd.** London, UK

Development Engineer

- Part of the hardware engineering team, developing a set-top box for interactive TV programming. Helped support initial production runs
- Working alone, I designed an ASIC to significantly reduce the cost of the handset for the interactive TV home unit

1994-1996 **Switched Reluctance Drives, Ltd.** Leeds, UK

Development Engineer

- Part of the hardware engineering team, developing high power drives and machinery
- Experience in digital design from concept to silicon. Involved design, simulation, and production of synthesis and production vectors. Produced 'Right First Time Silicon'. FPGAs used for emulation

Non-Career Experience

2000-2009 **Folsom Street Events** San Francisco, CA

Board President and Event Manager

- Board President of an extremely active working board for a non-profit organization producing events from 2000 people to 400,000 people
- Directly manage a staff of 2, board of 10, associate board of 9 and volunteer base of 450
- Doubled the size of the board from 5 members to 10 members
- More than doubled the size of the associate members (11)
- Managed annual board planning retreats and a new associates retreat
- Revised by-laws and created manuals for personnel and finance

- Grew the budget (with overall responsibility) to over \$1.2 million with eight annual events
- Directed new events, and improved existing events
- Expanded the Folsom brand with trademark rights in the US, Canada, EU, and AU with a licensing agreement for an EU event
- Took the agency through a successful 25TH anniversary
- Increased philanthropy with nearly half all charitable giving – nearly \$2 of \$4 million since becoming board president. Approximately \$350K given away annually
- Was responsible for the overall event and site management
- Enabled the organization to employ a full time staff

2000-Present Synopsys Users Group (SNUG) San Jose, CA

Technical Committee Member and Past Technical Chairman

- Technical chairman of SNUG for 3 years, helping drive the technical program as well as implementing and innovating new ideas
- General committee member responsible for paper reviewing

2000-Present International Test Conference (ITC)

Paper Reviewer

- General technical paper reviewer for the world’s largest test conference

2001-Present Large Non-Profit Event San Francisco, CA

Beverage Manager

- Beverage manager for a large (800K person) outdoor non-profit event
- Responsible for the event logistics, warehousing, inventory, delivery and documentation to support 45 bars over a two day event
- Developed and implemented a full training system for all of the volunteers in the safe service of alcohol (to meet ABC requirements), as well as general bar operation
- Manage all the staff (7), volunteer (400) and contracted labor (10), involved in the implementation of the beverage plan
- Produce full accounting, wrap-up reports and inventory reports

Patents

US Patent 6100823 “Single sensor position encoder providing two levels of resolution”
 US Patent 6301243 “Method and apparatus for transmitting data”
 US Patent 6515992 “Method and apparatus for input of data”

Education

B.Eng. (Hons) Electronic and Electrical Engineering School of Electronic and Electrical Engineering, Leeds University. **Major:** Power Electronics and Drives. Dissertation: Construction of a GPS receiver.

References

References are available upon request.